University of Fort Hare
Together in Excellence

PHY 313

DIGITAL ELECTRONICS

MAIN EXAMINATION

MAY/JUNE 2023

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TIME : 3 hours`

SUBJECT : DIGITAL ELECTRONICS

MARKS : 100

This paper consists of **THREE** pages including the cover page

INTERNAL EXAMINER

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EXTERNAL EXAMINER

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INSTRUCTIONS

ANSWER ALL QUESTIONS

QUESTION 1 {25 marks}

1.1. Simplify the logic circuit shown in Figure1. [8]

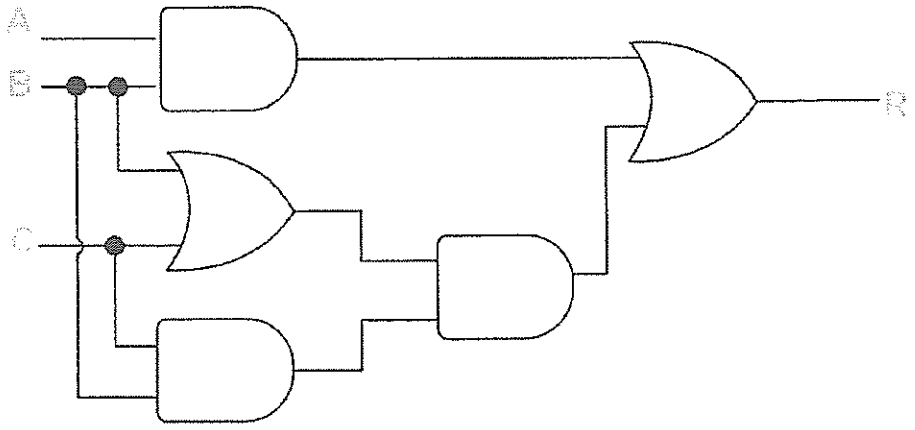

Figure 1: Logic gates

1.2. Find the Boolean algebra expression for the following system. [5]

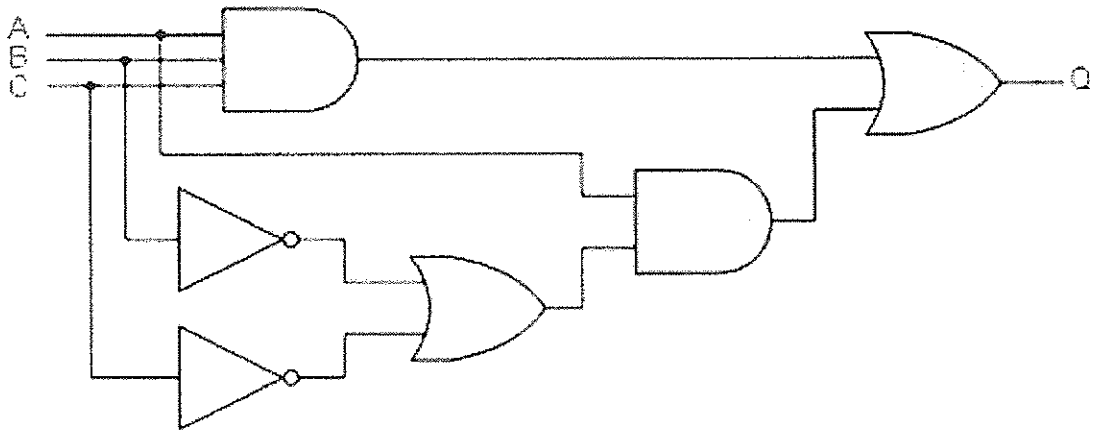

Figure 2: Logic circuit

1.3. Design a logic circuit that has three inputs, *A*, *B*, and *C*, and whose output will be HIGH only when the majority of the inputs are HIGH. [12]

QUESTION 2 {25 marks}

2.1. Simplify the Boolean function **F = AB + (AC)' + AB'C(AB + C).** [5]

2.2. Consider the function: $Y = (A \cdot B) + \overline{(\overline{A \cdot C})} \cdot \overline{B}$

2.2.1. Draw a combinational logic circuit that implements this function. [5]

2.2.2. Draw a truth table for this function. [5]

2.2.3. Write a sum-of-products representation of **Y.** [5]

2.2.4. Write a product-of-sums representation of **Y.** [5]

QUESTION 3 {25 marks}

3.1. For a **Full Adder (FA):**

3.1.1. Construct its truth table. [5]

3.1.2 Deduce the logical function for **Sum (S)** and **carry output (Co)** from the truth table using **(SOP).** [8]

3.1.3 Draw a logic circuit to generate **Co** and S from the **FA.** [4]

3.2. A circuit uses NOR gates to form a logic function X given by:

$$X = \overline{A + B} + \overline{\overline{A} + \overline{C}}$$

Use De-Morgan's theorems to turn this into a form suitable for implementing solely in **NAND** gates and draw the circuit diagram. [8]

QUESTION 4 {25 marks}

4.1. Give differences between combinational and sequential logic circuit. [5]
4.2. Give differences between counters and shift registers in tabular form. [5]
4.3 Draw a truth table of a **JK** flip-flop. [5]
4.4 Construct an asynchronous binary counter using the J-K flip-flops. [10]
